Features

- 2.5 A maximum peak output current
- 2.0 A minimum peak output current
- 250 ns maximum propagation delay over temperature range
- 1.7A Active Miller Clamp. Clamp pin short to V_{EE} if not in used
- Miller Clamping
- Desaturation Detection
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- Open Collector Isolated fault feedback
- “Soft” IGBT Turn-off
- 100 ns maximum pulse width distortion (PWD)
- 50 kV/μs minimum common mode rejection (CMR) at V_{CM} = 1500 V
- I_{CC}(max) <4.5 mA maximum supply current
- Wide V_{CC} operating range: 15 V to 30 V over temperature range
- Wide operating temperature range: –40-110°C

Applications

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply(UPS)

Pb Reach RoHS

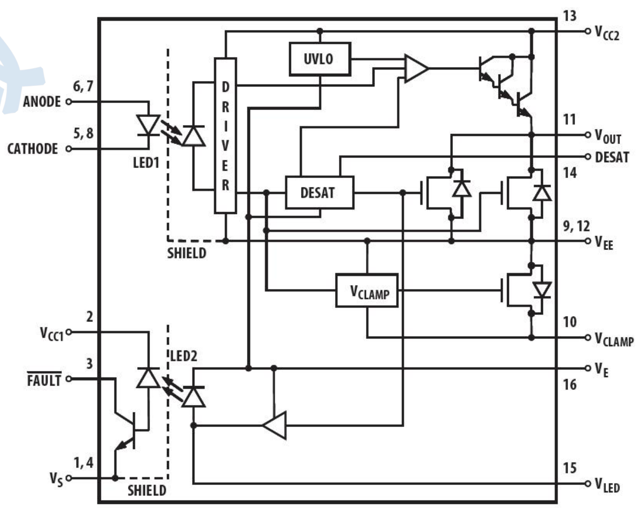
Description

The ICPL-332J contains a AlGaAs LED. The LED is optically coupled to an integrated circuit with a power output stage. ICPL-332J is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 150 A. For IGBTs with higher ratings, the ICPL-332J can be used to drive a discrete power stage which drives the IGBT gate.

The ICPL-332J has an insulation voltage of VIORM = 1414VPEA

Caution

It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

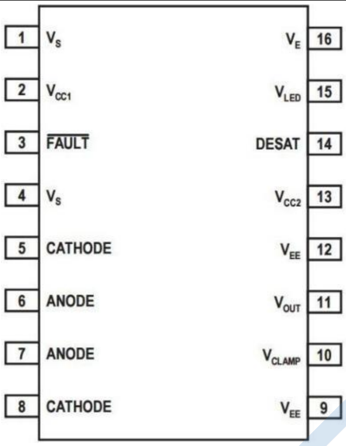


ORDERING INFORMATION

Outline	Part Number	Package	Marking	Packing	Packing Size	Quantity
	ICPL-332J-500E	SOP16	ICPL 332J /YYWW	Reel	13 "	1000

CONTENTS

PIN CONFIGURATION AND FUNCTIONS



Pin	Symbol	Description
1	V_S	Input Ground
2	V_{CC1}	Positive input supply voltage. (3.3 V to 5.5 V)
3	$\overline{FAULT}$	Fault output. $\overline{FAULT}$ changes from a high impedance state to a logic low output within 5 µs of the voltage on the DESAT pin exceeding an internal reference voltage of 6.5 V. $\overline{FAULT}$ output is an open collector which allows the $\overline{FAULT}$ outputs from all ICPL-332J in a circuit to be connected together in a “wired OR” forming a single fault bus for inter-facing directly to the micro-controller.
4	V_S	Input Ground
5	CATHODE	Cathode
6	ANODE	Anode
7	ANODE	Anode
8	CATHODE	Cathode
9	V_{EE}	Output supply voltage.
10	V_{CLAMP}	Miller clamp
11	V_{OUT}	Gate drive voltage output
12	V_{EE}	Output supply voltage.
13	V_{CC2}	Positive output supply voltage
14	DESAT	Desaturation voltage input. When the voltage on DESAT exceeds an internal reference voltage of 6.5 V while the IGBT is on, FAULT output is changed from a high impedance state to a logic low state within 5 µs.
15	V_{LED}	LED anode. This pin must be left unconnected for guaran- teed data sheet performance. (For optical coupling testing only)
16	V_E	Common (IGBT emitter) output supply voltage.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	Tstg	-55	125	℃	
Operating Temperature	T_A	-40	110	℃	2
Output IC Junction Temperature	TJ		125	℃	2
Average Forward Input Current	IF		20	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	VR		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	3
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	3
Positive Input Supply Voltage	V_{CC1}	-0.5	7.0	V	
FAULT Output Current	I_{FAULT}		8.0	mA	
FAULT Pin Voltage	V_{FAULT}	-0.5	V_{CC1}	V	
Total Output Supply Volta	$(V_{CC2} - V_{EE})$	-0.5	33	V	
Negative Output Supply Voltage	$(V_E - V_{EE})$	-0.5	15	V	6
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	-0.5	$33-(V_E-V_{EE})$	V	
Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V	
Peak Clamping Sinking Current	I_{Clamp}		1.7	A	
Miller Clamping Pin Voltage	V_{Clamp}	-0.5	V_{CC2}	V	
DESAT Voltage	V_{DESAT}	V_E	V_E+10	V	
Output IC Power Dissipation	P_O		600	mW	2
Input IC Power Dissipation	P_I		150	mW	2

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Min	Max	Units	Note
Operating Temperature	T_A	-40	110	°C	2
Total Output Supply Voltage	$(V_{CC2} - V_{EE})$	15	30	V	7
Negative Output Supply Voltage	$(V_E - V_{EE})$	0	15	V	4
Positive Output Supply Voltage	$(V_{CC2} - V_E)$	15	$30-(V_E-V_{EE})$	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	

ELECTRICAL OPTICAL CHARACTERISTICS

Unless otherwise noted, all typical values at T_a = 25°C, V_{CC2} - V_{EE} = 30V, V_E - V_{EE} = 0V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Note
FAULT Logic Low Output Voltage	V_{FAULTL}	-	0.01	0.4	V	I_{FAULT} = 1.1 mA, V_{CC1} = 5.5V	
		-	0.02	0.4	V	I_{FAULT} = 1.1 mA, V_{CC1} = 3.3V	
FAULT Logic High Output Current	I_{FAULTH}	-	0.01	0.5	µA	V_{FAULT} = 5.5 V, V_{CC1} = 5.5V	
		-	0.006	0.3	µA	V_{FAULT} = 3.3 V, V_{CC1} = 3.3V	
High Level Output Current	I_{OH}	-	-2	-0.5	A	V_O = V_{CC2} – 4	5
		-	-	-2.0	A	V_O = V_{CC2} – 15	3
Low Level Output Current	I_{OL}	0.5	2	-	A	V_O = V_{EE} + 2.5	5
		2.0	-	-	A	V_O = V_{EE} + 15	3
Low Level Output Current During Fault Condition	I_{OLF}	70	100	230	mA	V_{OUT} - V_{EE} = 14 V	6
High Level Output Voltage	V_{OH}	V_{CC}-0.5	V_{CC}-0.1	-	V	I_O = -650 µA	7,8,9,23
Low Level Output Voltage	V_{OL}	-	0.1	0.5	V	I_O = 100 mA	
Clamp Pin Threshold Voltage	V_{tClamp}	-	2.2	-	V		
Clamp Low Level Sinking Current	I_{CL}	0.35	1.0	-	A	V_O = V_{EE} + 2.5	
High Level Supply Current	I_{CC2H}	-	2.23	5	mA	I_O = 0 mA	9
Low Level Supply Current	I_{CC2L}	-	2.36	5	mA	I_O = 0 mA	
Blanking Capacitor Charging Current	I_{CHG}	0.13	-0.24	-0.33	mA	V_{DESAT} = 2 V	9,10
Blanking Capacitor Discharge Current	I_{DSCHG}	10	31	-	mA	V_{DESAT} = 7.0 V	
DESAT Threshold	V_{DESAT}	6	6.7	7.5	V	V_{CC2} -V_E >V_{UVLO-}	9
UVLO Threshold	V_{UVLO+}	10.5	11.5	12.5	V	V_O > 5 V	7,9,11
	V_{UVLO-}	9.2	10.5	11.1	V	V_O < 5 V	7,9,12
UVLO Hysteresis	(V_{UVLO+} - V_{UVLO-})	0.4	1	-	V		
Threshold Input Current Low to High	I_{FLH}	-	0.27	5	mA	I_O = 0 mA, V_O > 5 V	
Threshold Input Voltage High to Low	V_{FHL}	0.8	1.74	-	V		
Input Forward Voltage	V_F	1.6	2.0	2.4	V	I_F = 10 mA	
Input Reverse Breakdown Voltage	BV_R	5	-	-	V	I_R = 10 µA	
Input Capacitance	C_{IN}	-	70	-	pF	f = 1 MHz, V_F = 0 V	

SWITCHING SPECIFICATION

Unless otherwise noted, all typical values at T_a = 25°C, V_{CC2} - V_{EE} = 30V, V_E - V_{EE} = 0V; All Minimum/Maximum specifications are at Recommended Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions	Note
Propagation Delay Time to Output Low Level	t_{PHL}	50	94	250	ns	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{CC2} = 30 V	
Propagation Delay Time to Output High Level	t_{PLH}	50	97	250	ns		13,15
Pulse Width Distortion	PWD	-100	-	100	ns		14,17
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-150	-	150	ns		17,16
Rise Time	t_r	-	22	-	ns		
Fall Time	t_f	-	14	-	ns		
DESAT Sense to 90% VO Delay	$t_{DESAT(90\%)}$	-	0.1	0.5	µs	C_{DESAT} = 100pF, R_F=2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	19
DESAT Sense to 10% VO Delay	$t_{DESAT(10\%)}$	-	2.3	3	µs	C_{DESAT} = 100pF, R_F=2.1kΩ , Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	
DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$	-	0.2	0.5	µs	C_{DESAT} = 100 pF, R_F = 2.1 kΩ, C_F = Open, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	18
		-	0.8	-	µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, C_F = 1 nF, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$	-	0.15	-	µs	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	19
DESAT Input Mute	$t_{DESAT(MUTE)}$	5	-	-	µs	C_{DESAT} = 100pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC1} = 5.5V, V_{CC2} = 30 V	20
RESET to High Level FAULT Signal Delay	$t_{RESET(FAULT)}$	0.2	0.6	2.0	µs	C_{DESAT} = 100pF, RF = 2.1 kΩ,Rg = 10 Ω, Cg = 10 nF,V_{CC1} = 5.5V, V_{CC2} = 30 V	
RESET to High Level FAULT Signal Delay	$t_{RESET(FAULT)}$	0.2	0.6	2.5	µs	C_{DESAT} = 100pF, RF = 2.1 kΩ,Rg = 10 Ω, Cg = 10 nF,V_{CC1} = 3.3V, V_{CC2} = 30 V	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15	-	-	kV/µs	T_A = 25°C, I_F = 10 mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 15 pF	21
		50	-	-		T_A = 25°C, I_F = 1 mA V_{CM} =1500 V, V_{CC2} = 30 V, R_F =2.1 kΩ, C_F = 1 nF	21,26
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15	-	-	kV/µs	T_A = 25°C, V_F = 0 VV_{CM} = 1500 V, V_{CC2} = 30V,RF = 2.1kΩ, C_F = 15pF	22
		50	-	-		T_A = 25°C, V_F = 0 VV_{CM} = 1500 V, VCC2 = 30V,R_F = 2.1kΩ, C_F = 1nF	

Notes:

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at 10 mW/°C above 90°C. Input IC power dissipation does not require derating.
3. Maximum pulse width = 10 μs. This value is intended to allow for component tolerances for designs with I_O peak minimum = 1.0 A. Derate linearly from 2.0 A at +25°C to 1.5 A at +105°C. This compensates for increased I_{OPEAK} due to changes in V_{OL} over temperature.
4. This supply is optional. Required only when negative gate drive is implemented.
5. Maximum pulse width = 50 μs.
6. See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.
7. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5 V. For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
8. Maximum pulse width = 1.0 ms.
9. Once V_O of the ICPL-332J is allowed to go high (V_{CC2} - V_E > V_{UVLO+}), the DESAT detection feature of the ICPL-332J will be the primary source of IGBT protection. UVLO is needed to ensure D_{ESAT} is functional. Once V_{CC2} is increased from 0V to above V_{UVLO+}, DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-}. Thus, the DESAT detection and UVLO features of the ICPL-332J work in conjunction to ensure constant IGBT protection.
10. See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
11. This is the “increasing” (i.e. turn-on or “positive going” direction) of V_{CC2} - V_E
12. This is the “decreasing” (i.e. turn-off or “negative going” direction) of V_{CC2} - V_E
13. This load condition approximates the gate load of a 1200 V/75A IGBT.
14. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
15. As measured from IF to V_O.
16. The difference between t_{PHL} and t_{PLH} between any two ICPL-332J parts under the same test conditions.
17. As measured from ANODE, CATHODE of LED to V_{OUT}
18. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.

19. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
20. Auto Reset: This is the amount of time when V_{OUT} will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
21. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., $V_O > 15$ V or FAULT > 2 V).
22. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., $V_O < 1.0$ V or FAULT < 0.8 V).
23. To clamp the output voltage at V_{CC} - 3 $_{VBE}$, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 650 µA while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
24. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
25. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
26. Split resistors network with a ratio of 1:1 is needed at input LED1.

TYPICAL PERFORMANCE CURVES

Fig.1 IOH vs. Temperature

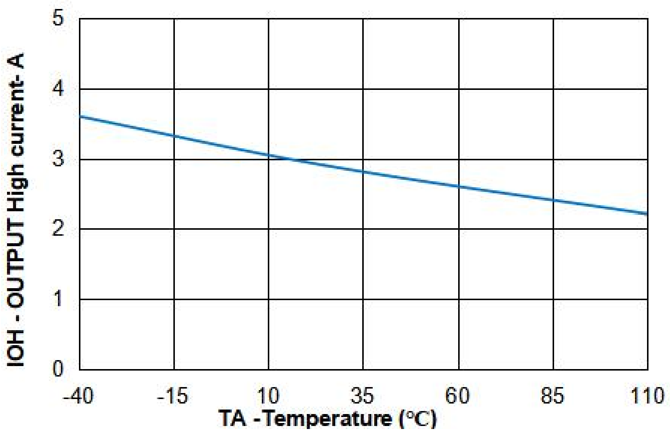


Fig.2 IOL vs. Temperature

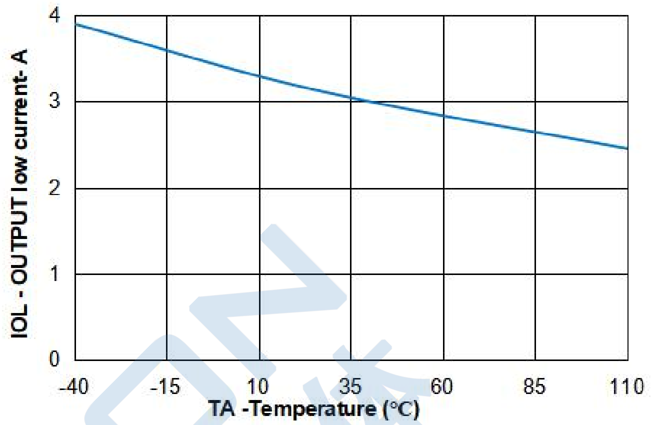


Fig.3 VOH vs. temperature

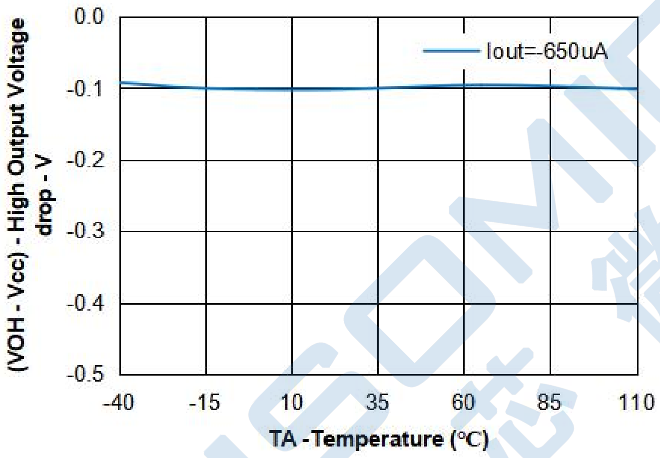


Fig.4 VOL vs. temperature

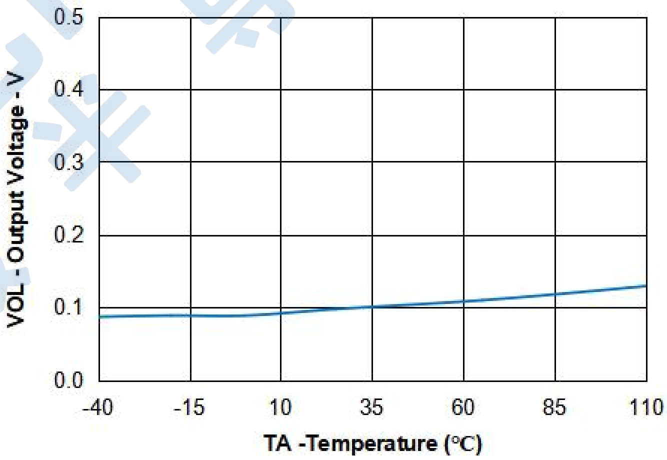


Fig.5 VOH vs. IOH

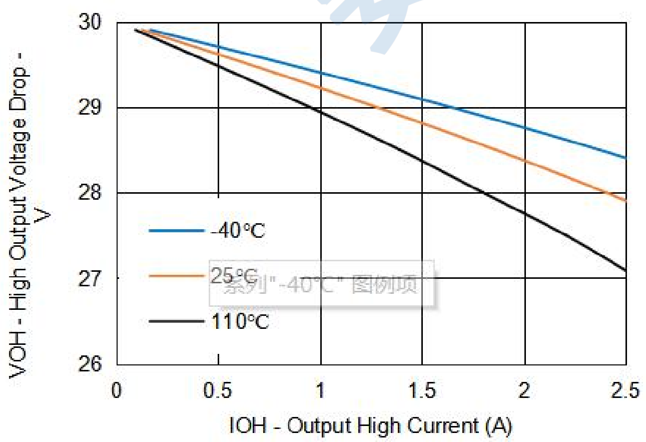


Fig.6 VOL vs. IOL

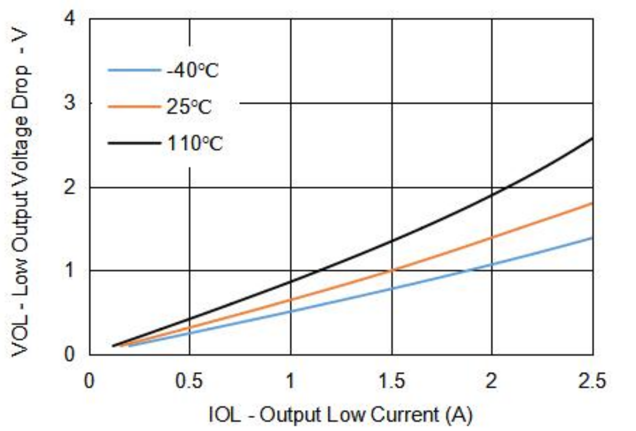


Fig.7 ICL vs. temperature

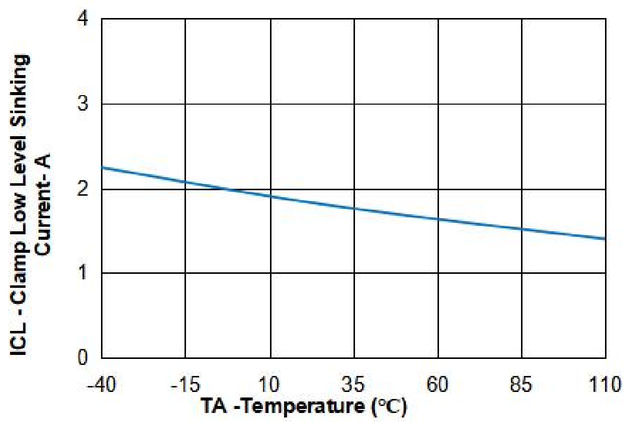


Fig.8 ICC2 vs. temperature

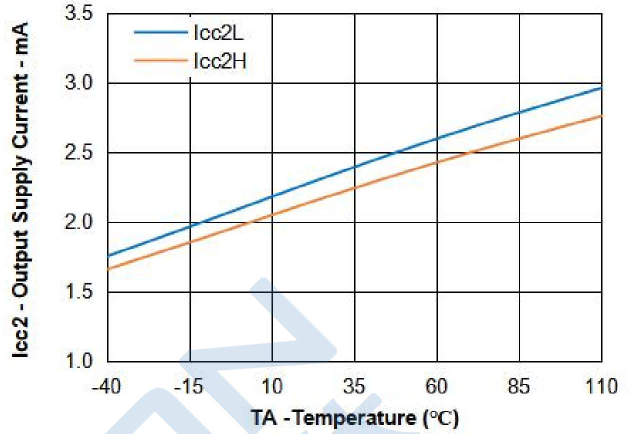


Fig. 9 ICC2 vs. VCC2

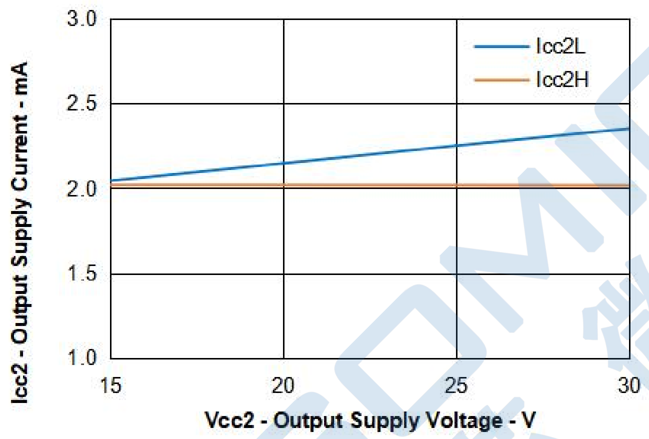


Fig.10 ICHG vs. temperature

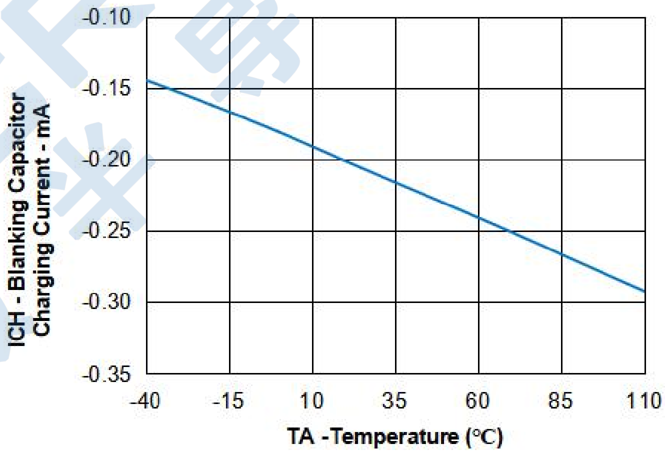


Fig.11 DESAT threshold vs. temperature

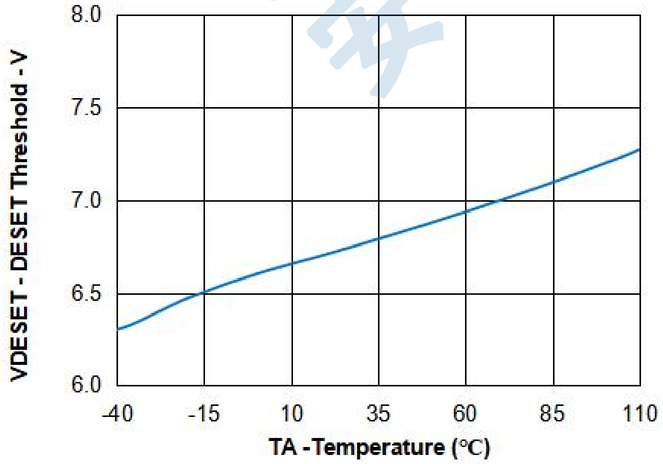


Fig.12 Propagation delay vs. temperature

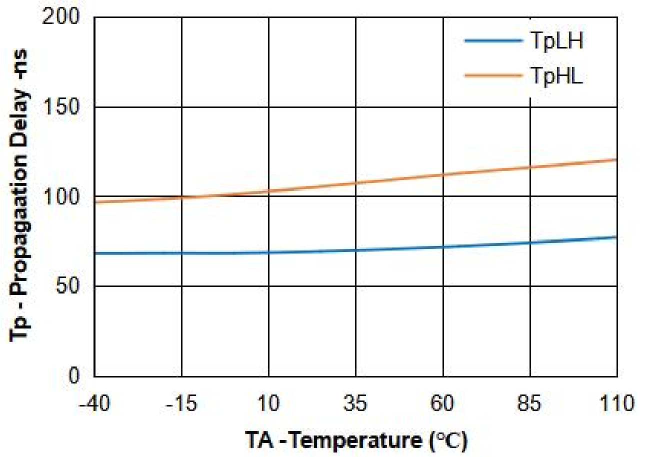


Fig.13 Propagation delay vs. supply voltage

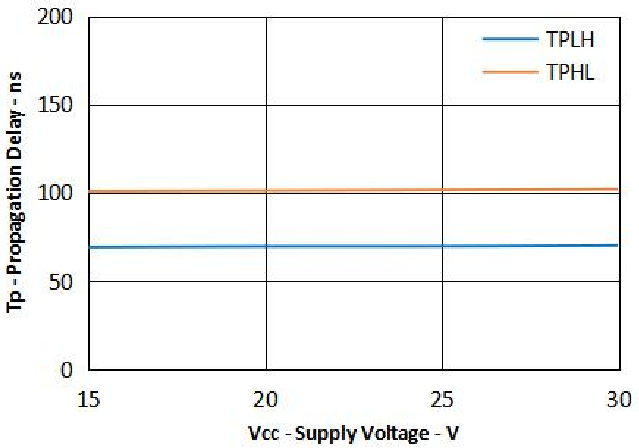


Fig.14 Propagation delay vs. RL

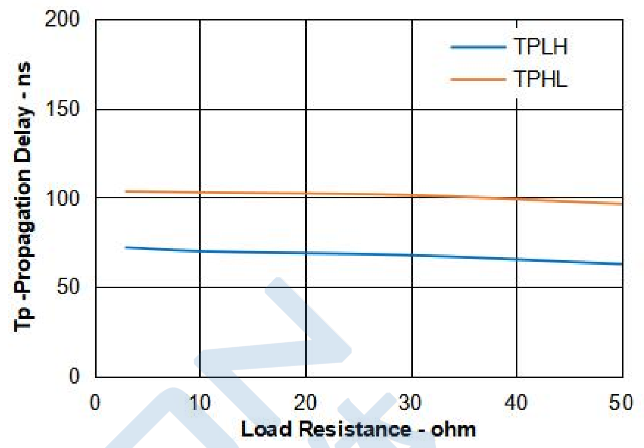


Fig.15 Propagation delay vs. CL

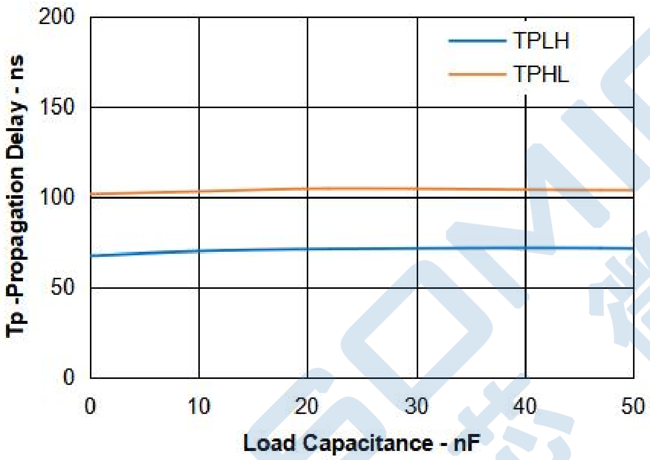


Fig.16 TDESAT90% vs. temperature

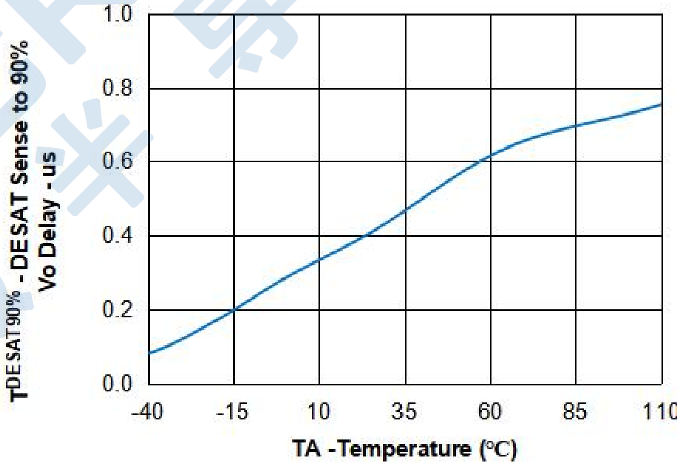


Fig.17 TDESAT10% vs. temperature

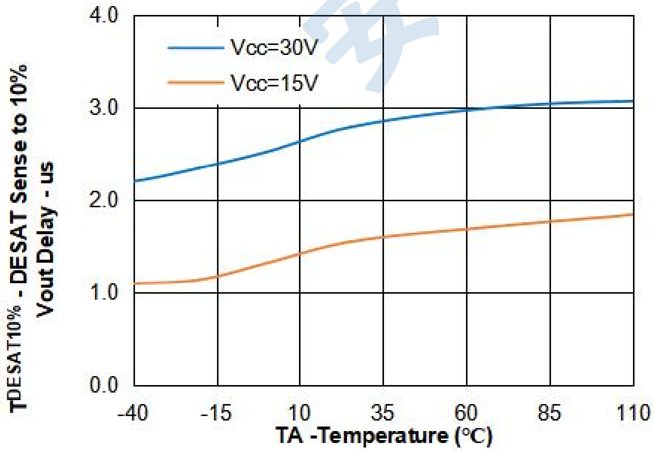


Fig.18 TDESAT10% vs. RL

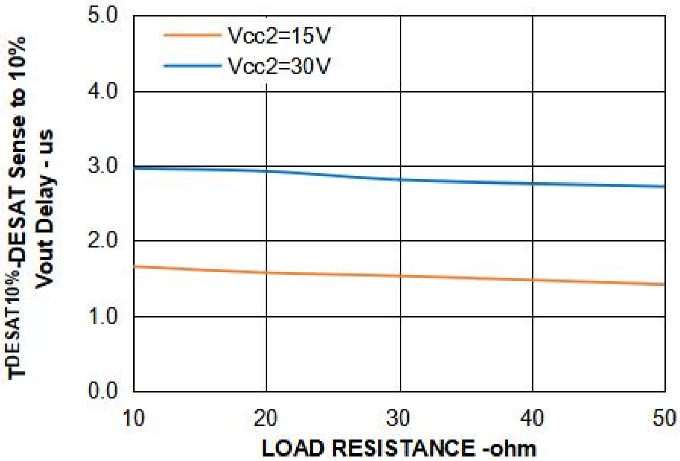
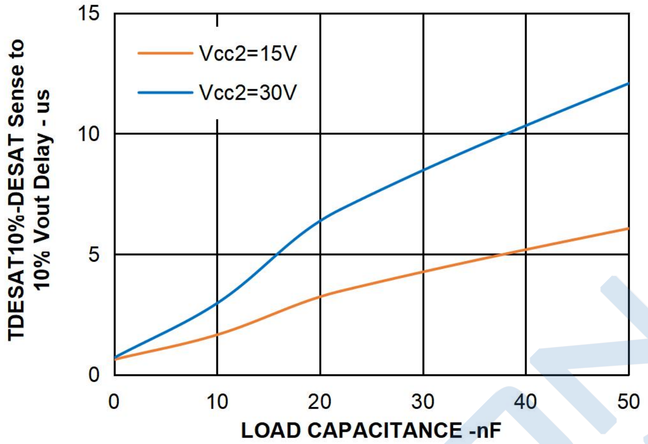


Fig.19 TDESAT10% vs. CL



TEST CIRCUITS

Fig.21 I_{OH} Pulsed test circuit

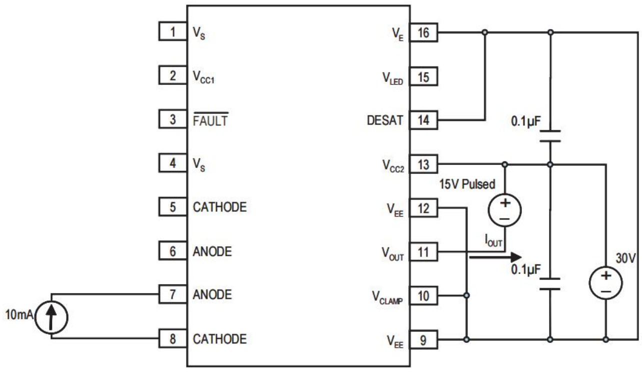


Fig.22 I_{OL} Pulsed test circuit

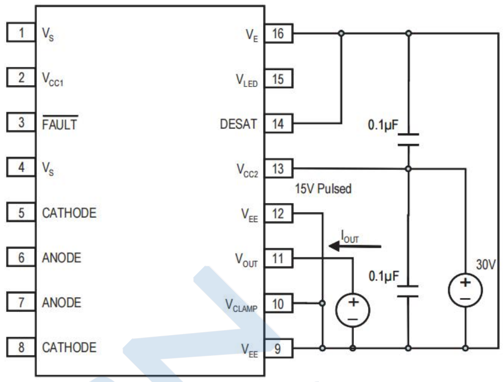


Fig.23 V_{OH} Pulsed test circuit

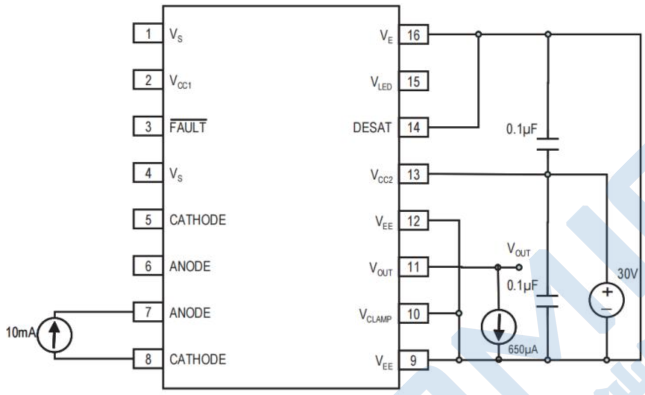


Fig.24 V_{OL} Pulsed test circuit

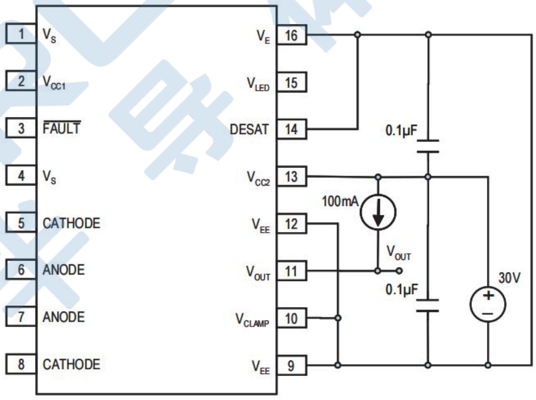


Fig.25 I_{CC2H} test circuit

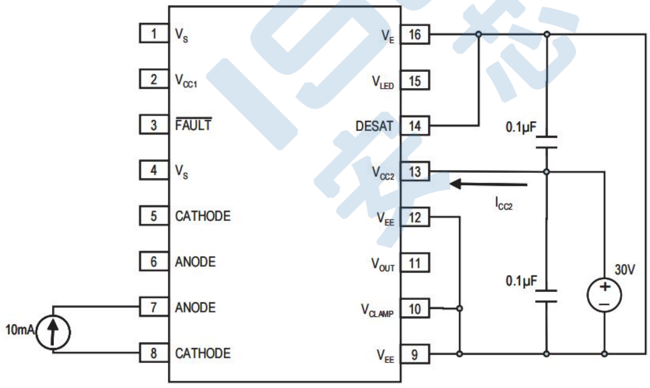


Fig.26 I_{CC2L} test circuit

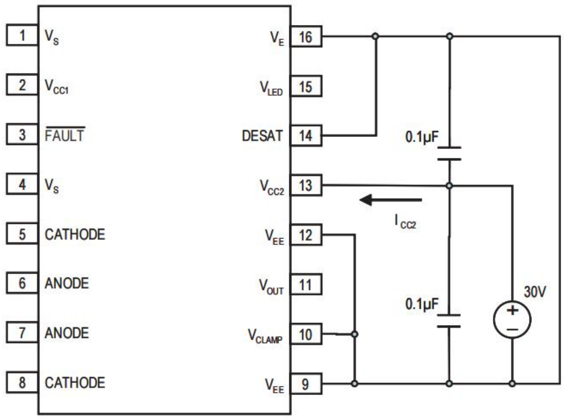


Fig.27 I_{CHG} Pulsed test circuit

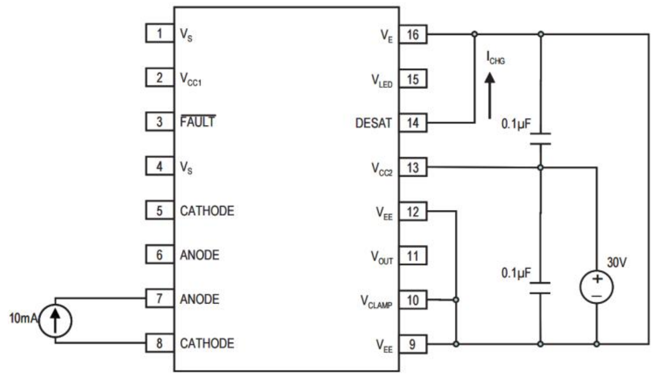


Fig.28 I_{DSCHG} test circuit

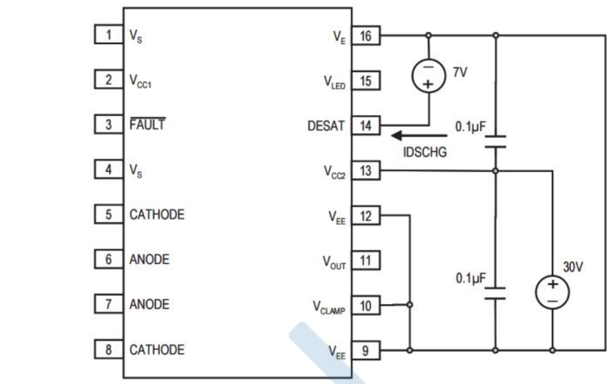


Fig.29 t_{PLH}, t_{PHL}, t_f, t_r, test circuit

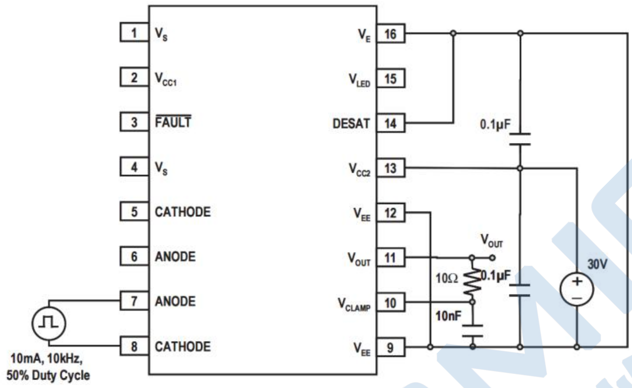


Fig.30 t_{DESAT} fault test circuit

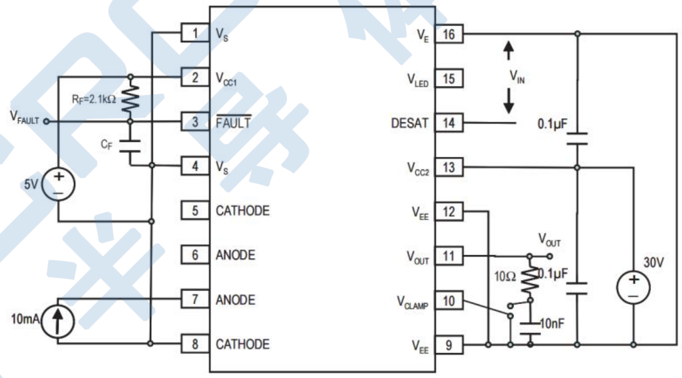


Fig.31 CMR Test circuit LED2 off

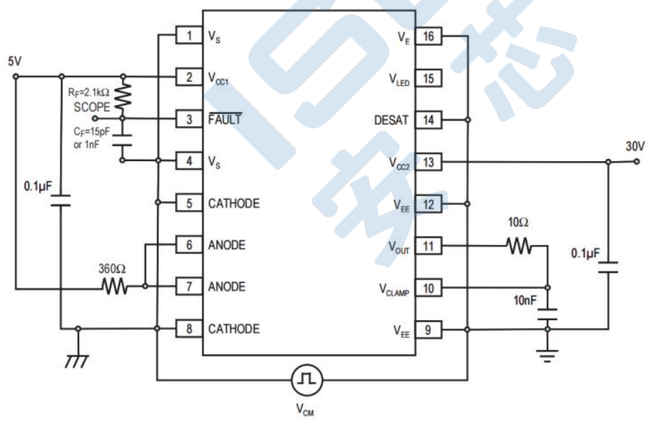


Fig.32 CMR Test Circuit LED2 on

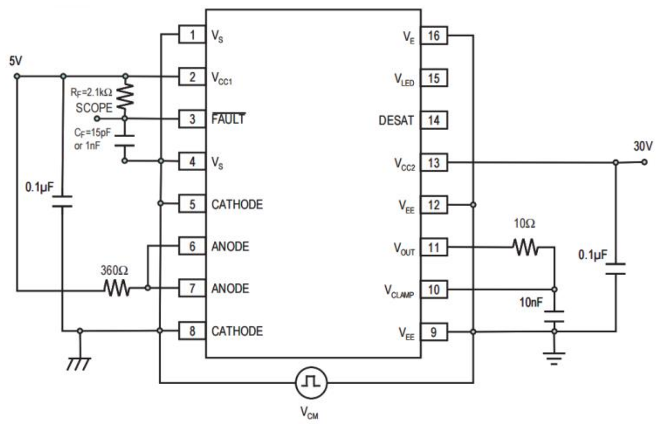


Fig.33 CMR Test circuit LED1 on

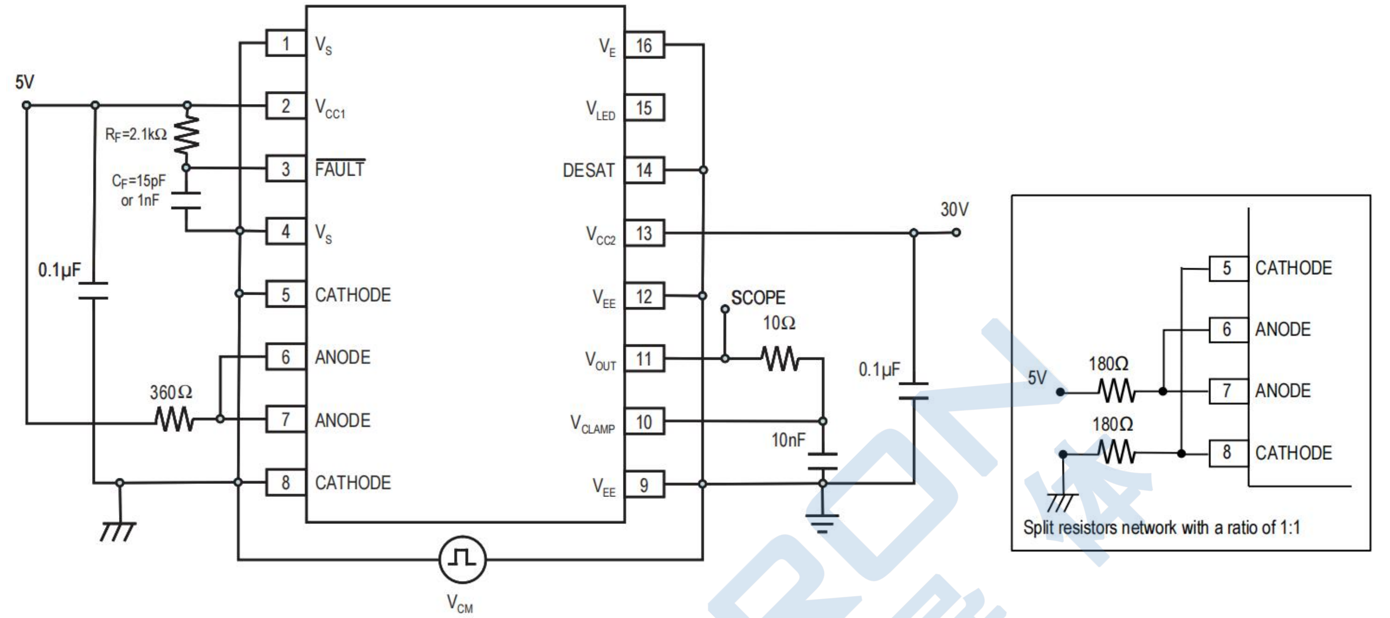
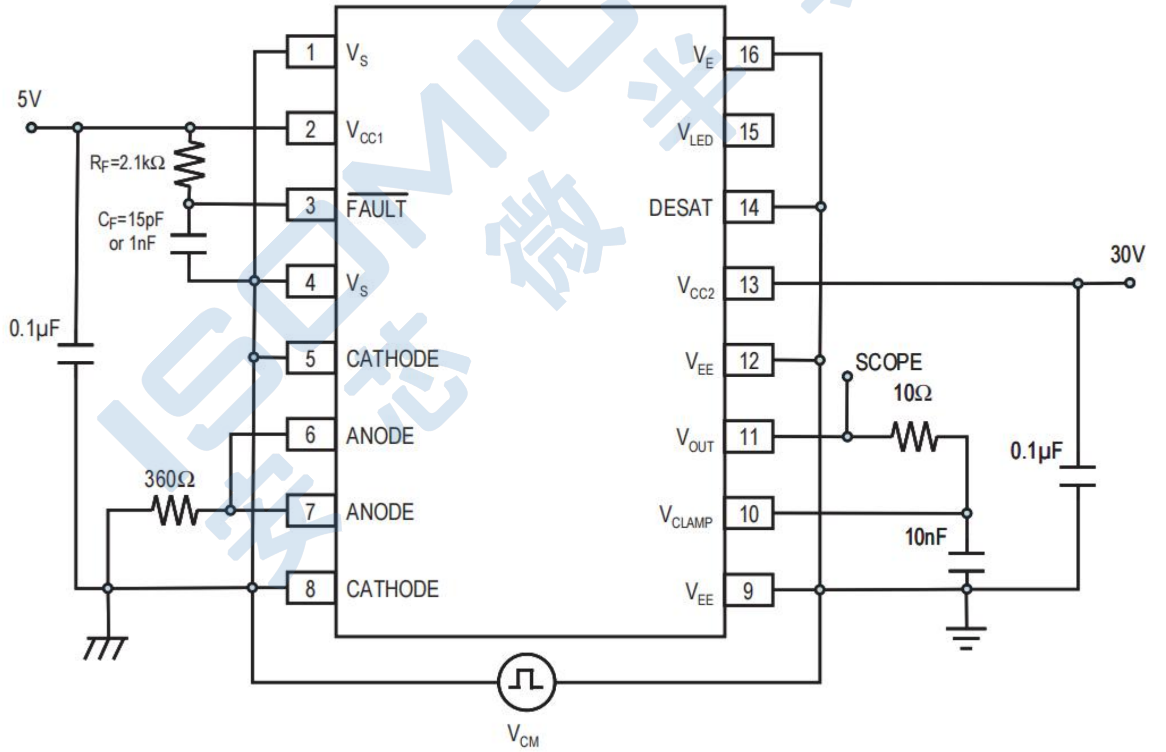


Fig.34 CMR Test Circuit LED1 off



Application Information Product Overview Description

The ICPL-332J is a highly integrated power control device that incorporates all the necessary components for a complete, isolated IGBT / MOSFET gate drive circuit with fault protection and feedback into one SO-16 package. Active Miller clamp function eliminates the need of negative gate drive in most application and allows the use of simple bootstrap supply for high side driver. An optically isolated power output stage drives IGBTs with power ratings of up to 150A and 1200V. A high speed internal optical link minimizes the propagation delays between the microcontroller and the IGBT while allowing the two systems to operate at very large common mode voltage differences that are common in industrial motor drives and other power switching applications. An output IC provides local protection for the IGBT to prevent damage during over current, and a second optical link provides a fully isolated fault status feedback signal for the microcontroller. A built in “watchdog” circuit, UVLO monitors the power stage supply voltage to prevent IGBT caused by insufficient gate drive voltages. This integrated IGBT gate driver is designed to increase the performance and reliability of a motor drive without the cost, size, and complexity of a discrete design.

Two light emitting diodes and two integrated circuits housed in the same SO-16 package provide the input control circuitry, the output power stage, and two optical channels. The output Detector IC is designed manufactured on a high voltage BiCMOS/Power DMOS process. The forward optical signal path, as indicated by LED1, transmits the gate control signal. The return optical signal path, as indicated by LED2, transmits the fault status feedback signal.

Under normal operation, the LED1 directly controls the IGBT gate through the isolated output detector IC, and LED2 remains off. When an IGBT fault is detected, the output detector IC immediately begins a “soft” shutdown sequence, reducing the IGBT current to zero in a controlled manner to avoid potential IGBT damage from inductive over voltages. Simultaneously, this fault status is transmitted back to the input via LED2, where the fault latch disables the gate control input and the active low fault output alerts the microcontroller.

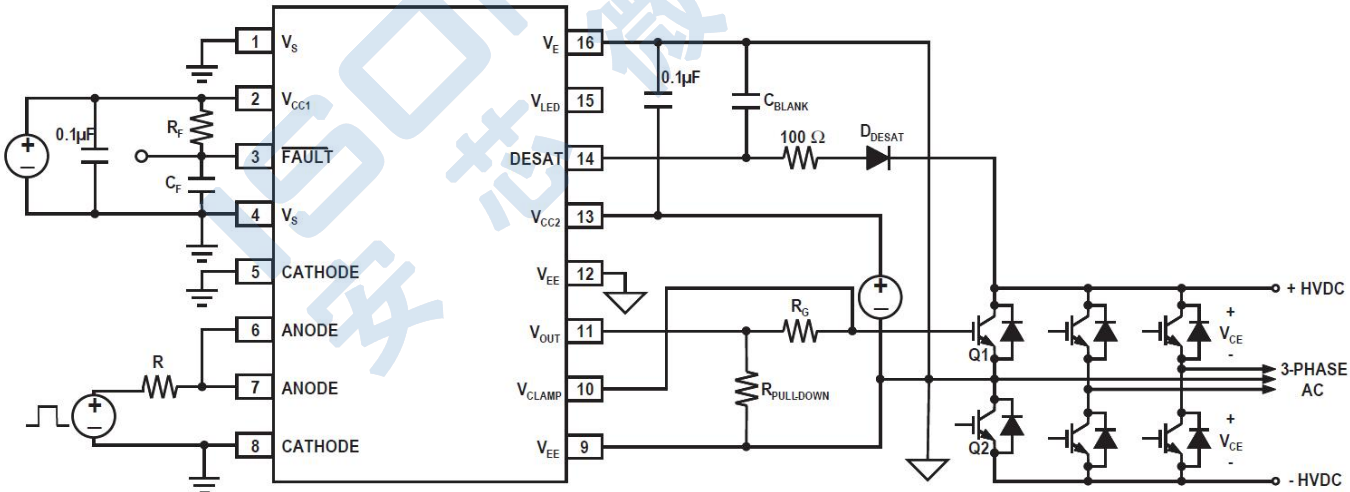
During power-up, the Under Voltage Lockout (UVLO) feature prevents the application of insufficient gate voltage to the IGBT, by forcing the ICPL-332J’s output low. Once the output is in the high state, the DESAT (VCE) detection feature of the ICPL-332J provides IGBT protection. Thus, UVLO and DESAT work in conjunction to provide constant IGBT protection.

Recommended Application Circuit

The ICPL-332J has an LED input gate control, and an open collector fault output suitable for wired 'OR' applications. The recommended application circuit shown in Figure 35 illustrates a typical gate drive implementation using the ICPL-332J. The following describes about driving IGBT. However, it is also applicable to MOSFET. Depending upon the MOSFET or IGBT gate threshold requirements, designers may want to adjust the V_{CC} supply voltage (Recommended V_{CC} = 17.5V for IGBT and 12.5V for MOSFET).

The two supply bypass capacitors (0.1 µF) provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, a low current (5mA) power supply suffices. The desaturation diode DDESAT 600V/1200V fast recovery type, trr below 75ns (e.g. ERA34-10) and capacitor CBLANK are necessary external components for the fault detection circuitry. The gate resistor RG serves to limit gate charge current and controls the IGBT collector voltage rise and fall times. The open collector fault output has a passive pull-up resistor RF (2.1 kΩ) and a 1000 pF filtering capacitor, CF. A 47kΩ pull down resistor RPULL-DOWN on V_{OUT} provides a predictable high level output voltage (V_{OH}). In this application, the IGBT gate driver will shut down when a fault is detected and fault reset by next cycle of IGBT turn on. Application notes are mentioned at the end of this datasheet.

Fig.35 Recommended application circuit (Single Supply) with desaturation detection and active Miller Clamp



Description of Operation-Normal Operation

During normal operation, V_{OUT} of the ICPL-332J is controlled by input LED current IF (pins 5, 6, 7 and 8), with the IGBT collector-to-emitter voltage being monitored through DESAT. The FAULT output is high. See Figure 36.

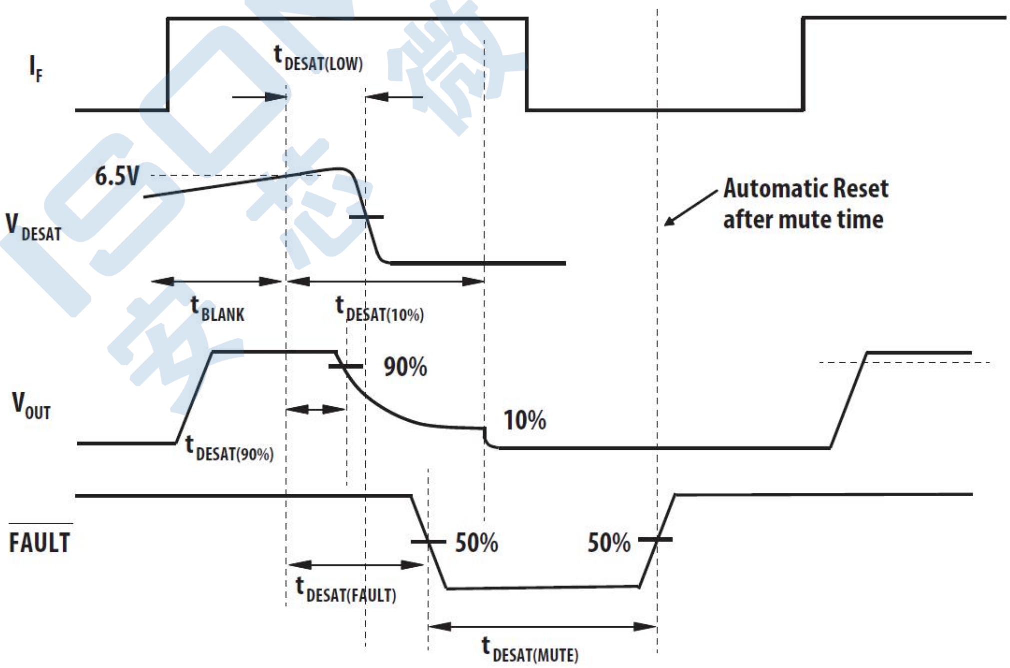
Fault Condition

The DESAT pin monitors the IGBT Vce voltage. When the voltage on the DESAT pin exceeds 6.5 V while the IGBT is on, V_{OUT} is slowly brought low in order to “softly” turn-off the IGBT and prevent large di/dt induced voltages. Also activated is an internal feedback channel which brings the FAULT output low for the purpose of notifying the micro-controller of the fault condition.

Fault Reset

Once fault is detected, the output will be muted for 5μs (minimum). All input LED signals will be ignored during the fault period to allow the driver to completely soft shut-down the IGBT. The fault mechanism can be reset by the next LED turn-on after the 5μs (minimum)mute time. See Figure 36.

Fig.36 Fault Timing diagram



Output Control

The outputs (V_{OUT} and FAULT) of the ICPL-332J are controlled by the combination of I_F, UVLO and a detected IGBT Desat condition. Once UVLO is not active (V_{CC2} - V_E > V_{UVLO}), V_{OUT} is allowed to go high, and the DESAT (pin 14) detection feature of the ICPL-332J will be the primary source of IGBT protection. Once V_{CC2} is increased from 0V to above V_{UVLO+}, DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-}. Thus, the DESAT detection and UVLO features of the ICPL-332J work in conjunction to ensure constant IGBT protection.

I_F	UVLO(V_{CC2}-V_E)	DESAT Function	FAULT Output	VOUT
ON	Active	Not Active	High	Low
ON	Not Active	Active (with DESAT fault)	Low (FAULT)	Low
ON	Not Active	Not Active (no DESAT fault)	High (or no fault)	High
OFF	Active	Not Active	High	Low
OFF	Not Active	Not Active	High	Low

Desaturation Detection and High Current Protection

The ICPL-332J satisfies these criteria by combining a high speed, high output current driver, high voltage optical isolation between the input and output, local IGBT desaturation detection and shut down, and an optically isolated fault status feedback signal into a single 16-pin surface mount package.

The fault detection method, which is adopted in the ICPL-332J is to monitor the saturation (collector) voltage of the IGBT and to trigger a local fault shutdown sequence if the collector voltage exceeds a predetermined threshold. A small gate discharge device slowly reduces the high short circuit IGBT current to prevent damaging voltage spikes. Before the dissipated energy can reach destructive levels, the IGBT is shut off. During the off state of the IGBT, the fault detect circuitry is simply disabled to prevent false 'fault' signals.

The alternative protection scheme of measuring IGBT current to prevent desaturation is effective if the short circuit capability of the power device is known, but this method will fail if the gate drive voltage decreases enough to only partially turn on the IGBT. By directly measuring the collector voltage, the ICPL-332J limits the power dissipation in the IGBT even with insufficient gate drive voltage. Another more subtle advantage of the desaturation detection method is that power dissipation in the IGBT is monitored, while the current sense method relies on a preset current threshold to predict the safe limit of operation. Therefore, an overly conservative over current threshold is not needed to protect the IGBT.

Slow IGBT Gate Discharge during Fault Condition

When a desaturation fault is detected, a weak pull-down device in the ICPL-332J output drive stage will turn on to 'softly' turn off the IGBT. This device slowly discharges the IGBT gate to prevent fast changes in drain current that could cause damaging voltage spikes due to lead and wire inductance. During the slow turn off, the large output pull-down device remains off until the output voltage falls below V_{EE} + 2 Volts, at which time the large pull down device clamps the IGBT gate to V_{EE}.

DESAT Fault Detection Blanking Time

The DESAT fault detection circuitry must remain disabled for a short time period following the turn-on of the IGBT to allow the collector voltage to fall below the DESAT threshold. This time period, called the DESAT blanking time is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor.

The nominal blanking time is calculated in terms of external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}) as $t_{BLANK} = C_{BLANK} \times V_{DESAT} / I_{CHG}$. The nominal blanking time with the recommended 100pF capacitor is 100pF * 6.5V / 240μA = 2.7μsec. The capacitance value can be scaled slightly to adjust the blanking time, though a value smaller than 100 pF is not recommended. This nominal blanking time represents the longest time it will take for the ICPL-332J to respond to a DESAT fault condition. If the IGBT is turned on while the collector and emitter are shorted to the supply rails (switching into a short), the soft shut-down sequence will begin after approximately 3 μsec. If the IGBT collector and emitter are shorted to the supply rails after the IGBT is already on, the response time will be much quicker due to the parasitic parallel capacitance of the DESAT diode. The recommended 100pF capacitor should provide adequate blanking as well as fault response times for most applications.

Under Voltage Lockout

The ICPL-332J Under Voltage Lockout (UVLO) feature is designed to prevent the application of insufficient gate voltage to the IGBT by forcing the ICPL-332J output low during power-up. IGBTs typically require gate voltages of 15V to achieve their rated $V_{CE(ON)}$ voltage. At gate voltages below 13V typically, the $V_{CE(ON)}$ voltage increases dramatically, especially at higher currents. At very low gate voltages (below 10V), the IGBT may operate in the linear region and quickly overheat. The UVLO function causes the output to be clamped whenever insufficient operating supply (V_{CC2}) is applied. Once V_{CC2} exceeds V_{UVLO+} (the positive-going UVLO threshold), the UVLO clamp is released to allow the device output to turn on in response to input signals. As V_{CC2} is increased from 0 V (at some level below V_{UVLO+}), first the DESAT protection circuitry becomes active. As V_{CC2} is further increased (above V_{UVLO+}), the UVLO clamp is released. Before the time the UVLO clamp is released, the DESAT protection is already active. Therefore, the UVLO and DESAT Fault detection feature work together to provide seamless protection regardless of supply voltage (V_{CC2}).

Active Miller Clamp

A Miller clamp allows the control of the Miller current during a high d_V/dt situation and can eliminate the use of a negative supply voltage in most of the applications. During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2V (relative to V_{EE}). The clamp voltage is V_{OL}+2.5V typ for a Miller current up to 1100mA. The clamp is disabled when the LED input is triggered again.

Other Recommended Components

The application circuit in Figure 33 includes an output pull-down resistor, a DESAT pin protection resistor, a FAULT pin capacitor, and a FAULT pin pullup resistor and Active Miller Clamp connection.

Output Pull-Down Resistor

During the output high transition, the output voltage rapidly rises to within 3 diode drops of V_{CC2}. If the output current then drops to zero due to a capacitive load, the output voltage will slowly rise from roughly V_{CC2}-3(V_{BE}) to V_{CC2} within a period of several microseconds. To limit the output voltage to V_{CC2}-3(V_{BE}), a pull-down resistor, RPULL-DOWN between the output and V_{EE} is recommended to sink a static current of several 650 μA while the output is high. Pull-down resistor values are dependent on the amount of positive supply and can be adjusted according to the formula, Rpull-down = [V_{CC2}-3 * (V_{BE})] / 650 μA.

DESAT Pin Protection Resistor

The freewheeling of flyback diodes connected across the IGBTs can have large instantaneous forward voltage transients which greatly exceed the nominal forward voltage of the diode. This may result in a large negative voltage spike on the DESAT pin which will draw substantial current out of the driver if protection is not used. To limit this current to levels that will not damage the driver IC, a 100 ohm resistor should be inserted in series with the DESAT diode. The added resistance will not alter the DESAT threshold or the DESAT blanking time.

Fig.37 Output pull-down resistor.

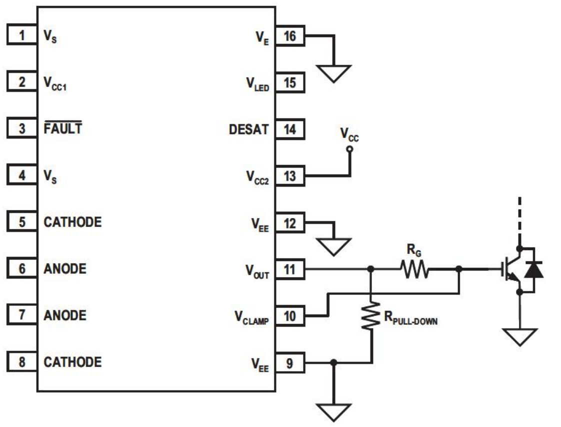
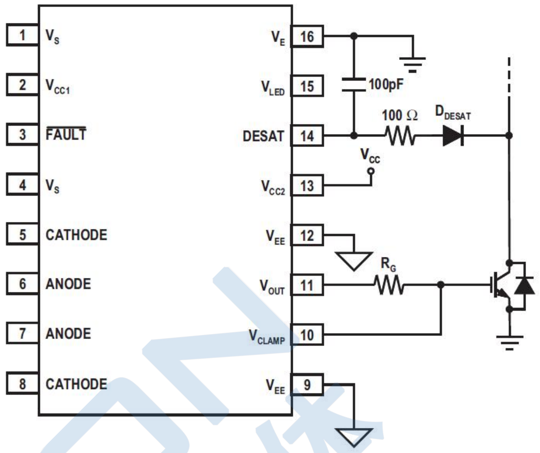


Fig.38 DESAT pin protection



Capacitor on FAULT Pin for High CMR

Rapid common mode transients can affect the fault pin voltage while the fault output is in the high state. A 1000 pF capacitor should be connected between the fault pin and ground to achieve adequate CMOS noise margins at the specified CMR value of 50 kV/μs.

Pull-up Resistor on FAULT Pin

The FAULT pin is an open collector output and therefore requires a pull-up resistor to provide a high-level signal. Also the FAULT output can be wire 'OR'ed together with other types of protection (e.g. over-temperature, over-voltage, over-current) to alert the microcontroller.

Other Possible Application Circuit (Output Stage)

Fig.39 IGBT drive with negative gate drive, external booster and desaturation detection (V_{CLAMP} should be connected to V_{EE} when it is not used) V_{CLAMP} is used as secondary gate discharge path. * indicates component required for negative gate drive topology

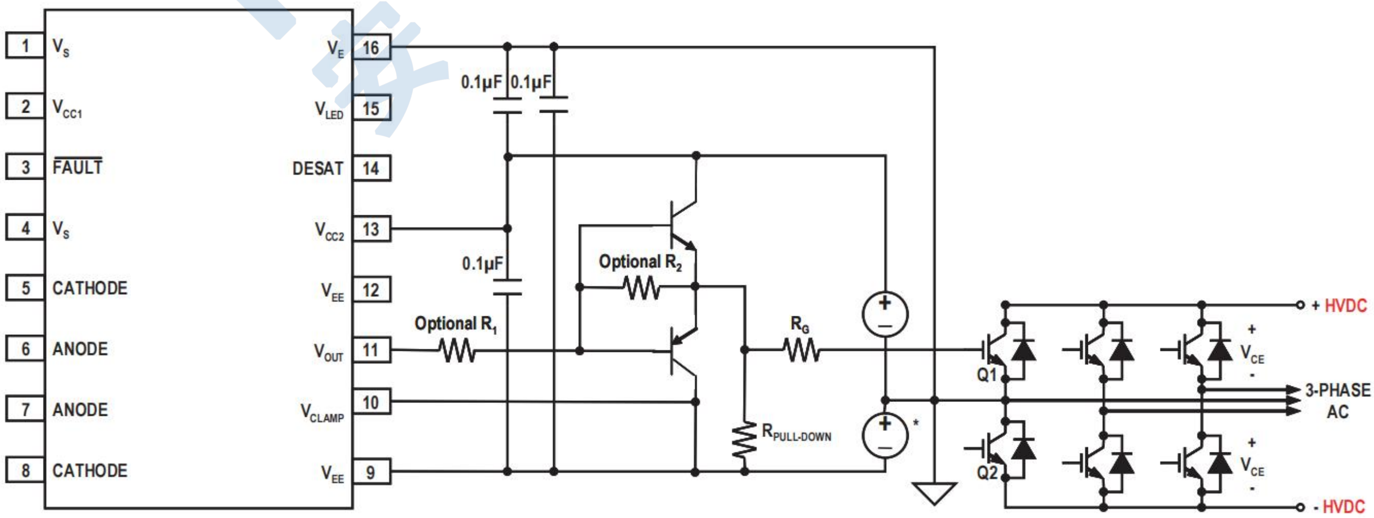
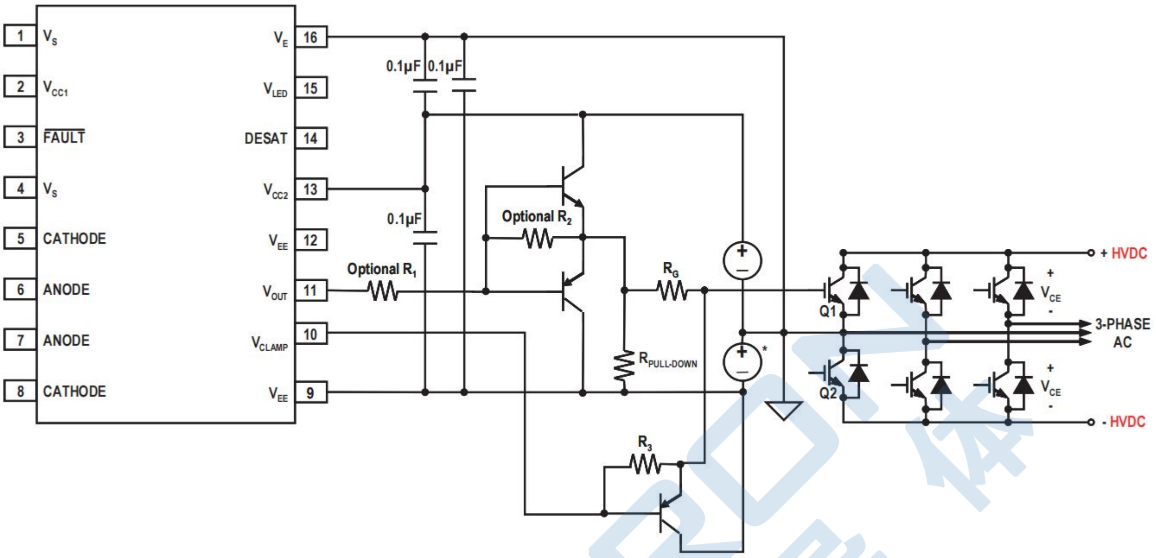


Fig.40 Large IGBT drive with negative gate drive, external booster. V_{CLAMP} control secondary discharge path for higher power application.



Thermal Model

The ICPL-332J is designed to dissipate the majority of the heat through pins 1, 4, 5 & 8 for the input IC and pins 9 &12 for the output IC. (There are two VEE pins on the output side, pins 9 and 12, for this purpose.) Heat flow through other pins or through the package directly into ambient are considered negligible and not modeled here. In order to achieve the power dissipation specified in the absolute maximum specification, it is imperative that pins 5, 9, and 12 have ground planes connected to them. As long as the maximum power specification is not exceeded, the only other limitation to the amount of power one can dissipate is the absolute maximum junction temperature specification of 125°C. The junction temperatures can be calculated with the following equations:

$T_{ji} = Pi\ (\theta i5 + \theta 5A) + T_a$

$T_{jo} = Po\ (\theta o9,12 + \theta 9,12A) + T_a$

Where Pi = power into input IC and Po = power into output IC. Since θ5A and θ9,12A are dependent on PCB layout and airflow, their exact number may not be available. Therefore, a more accurate method of calculating the junction temperature is with the following equations:

$T_{ji} = Pi\theta i5 + TP5$

$Tj_o = Po\theta o9,12 + TP9,12$

These equations, however, require that the pin 5 and pins 9, 12 temperatures be measured with a thermal couple on the pin at the ICPL-332J package edge.

If the calculated junction temperatures for the thermal model in Figure 38 is higher than 125°C, the pin temperature for pins 9 and 12 should be measured (at the package edge) under worst case operating environment for a more accurate estimate of the junction temperatures.

T_{ji} = junction temperature of input side IC

T_{jo} = junction temperature of output side IC TP5 = pin 5 temperature at package edge

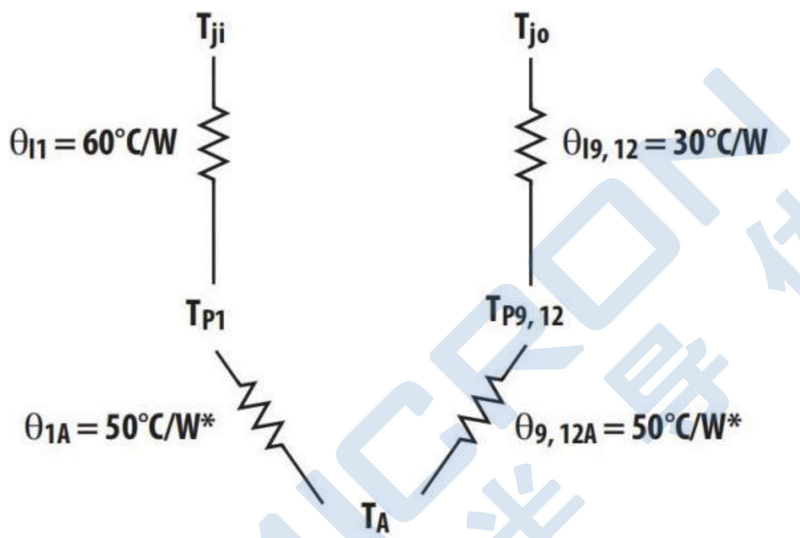
TP9, 2 = pin 9 and 12 temperature at package edge

θI5 = input side IC to pin 5 thermal resistance

θo9,12 = output side IC to pin 9 and 12 thermal resistance

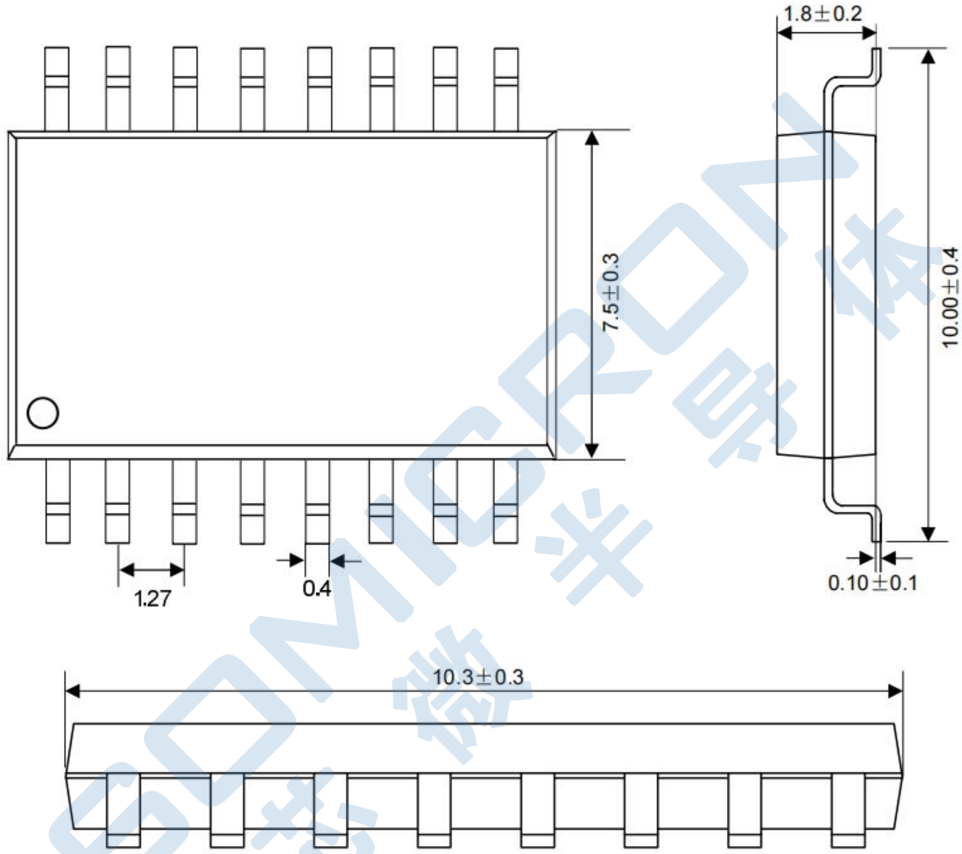
θ5A = pin 5 to ambient thermal resistance
θ9,12A = pin 9 and 12 to ambient thermal resistance
*The θ5A and θ9,12A values shown here are for PCB layouts with reasonable air flow. This value may increase or decrease by a factor of 2 depending on PCB layout and/or airflow.

Fig.38 ICPL-332J Thermal Model



PACKAGE DIMENSIONS

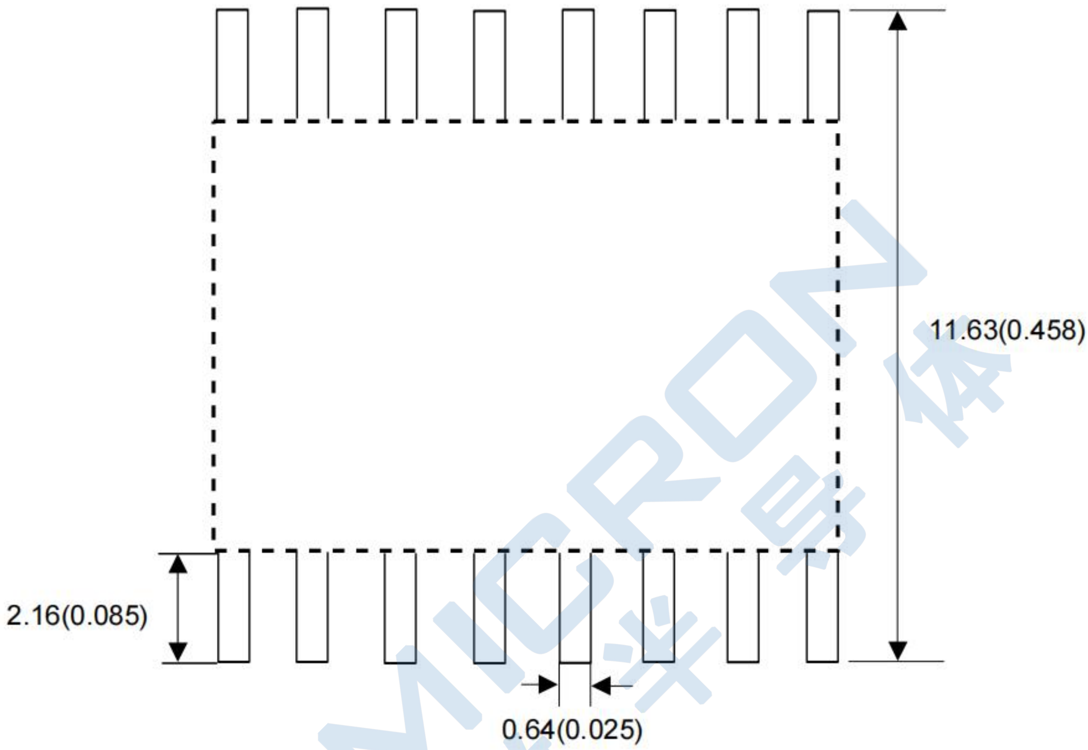
Surface Mount (Low Profile) Lead Forming (SL Type)



- **Dimensions in mm unless otherwise stated**

RECOMMENDED SOLDER MASK

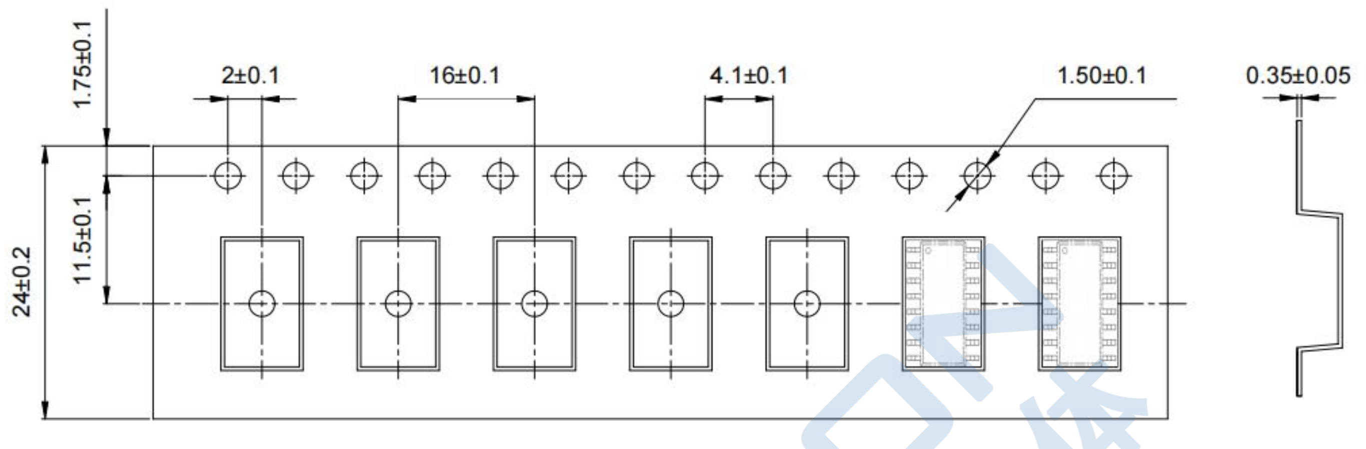
Surface Mount (Low Profile) Lead Forming



- **Dimensions in mm unless otherwise stated**

CARRIER TAPE SPECIFICATIONS

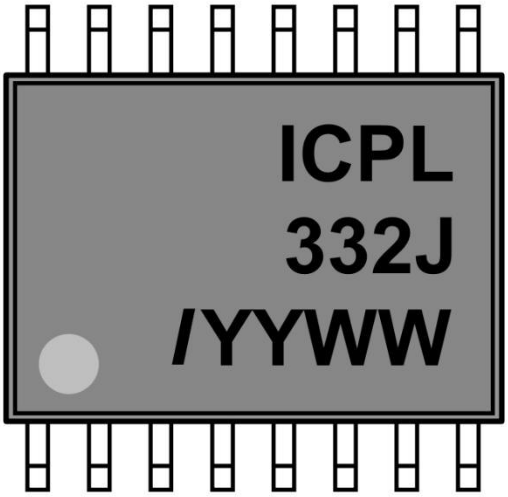
Option SOP16



- **Dimensions in mm unless otherwise stated**

ORDERING AND MARKING INFORMATION

Marking Information



ICPL	:	Company Abbr.
332J	:	Part Number
/	:	ISOMICRON
YY	:	Fiscal Year
WW	:	Work Week

Order Code

ICPL – 332J - 5 0 0 E

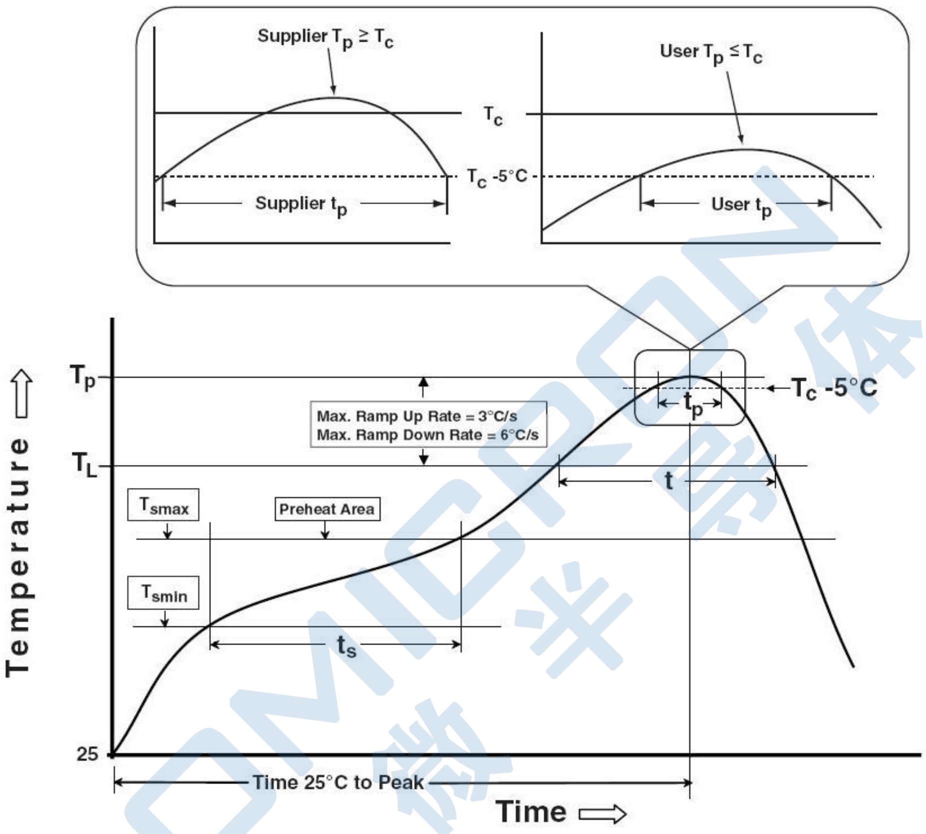
- **Company Abbr.** ← ICPL
- **Part Number** ← 332J
- **Lead Forming** ← 5
  5: SM-SL
- **Performance** ← 0
  0: Normal
  1: Enhanced
- **None** ← 0
- **Halogen Free** ← E
  E: Halogen-free,Lead-free
  Z: Halogen, Lead-free

Packing Quantity

Option	Quantity	Quantity	Quantity – Outer box
SM-SL	1000 Units/Reel	2	5 Inner box/Outer box = 10K Units

REFLOW INFORMATION

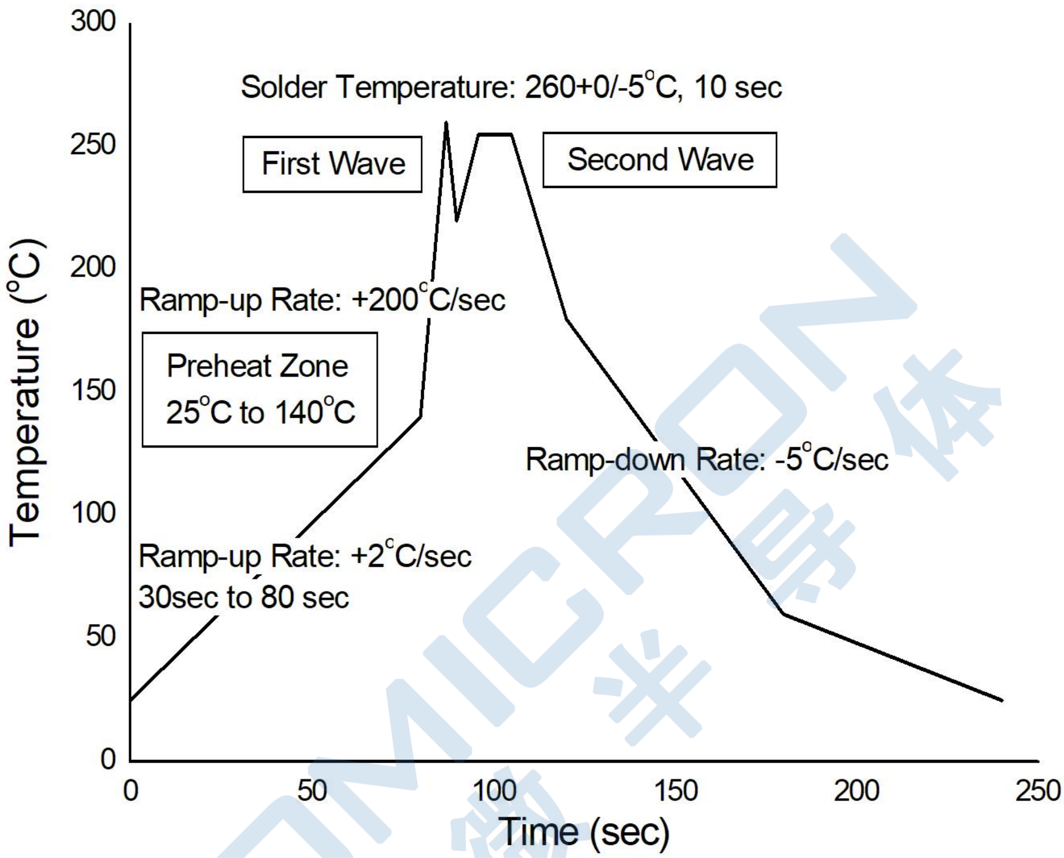
Reflow Profile



Profile Feature	Sn-Pb Assembly Profile	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	100	150°C
Temperature Max. (Tsmax)	150	200°C
Time (ts) from (Tsmin to Tsmax)	60-120 seconds	60-120 seconds
Ramp-up Rate (tL to tP)	3°C/second max.	3°C/second max.
Liquidous Temperature (TL)	183°C	217°C
Time (tL) Maintained Above (TL)	60 – 150 seconds	60 – 150 seconds
Peak Body Package Temperature	235°C +0°C / -5°C	260°C +0°C / -5°C
Time (tP) within 5°C of 260°C	20 seconds	30 seconds
Ramp-down Rate (TP to TL)	6°C/second max	6°C/second max
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

TEMPERATURE PROFILE OF SOLDERING

Wave Soldering (JESD22-A111 Compliant)



Hand Soldering By Soldering Iron	
Soldering Temperature	380+0/-5°C
Soldering Time	3 sec max.

- **One time soldering is recommended for all soldering method.**
- **Do not solder more than three times for IR reflow soldering.**

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- This product is not intended to be used for military, aircraft, medical, life sustaining or lifesaving applications or any other application which can result in human injury or death.
- Please contact ISOMICRON sales agent for special application request.
- Immerge unit’s body in solder paste is not recommended.
- Parameters provided in datasheets may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated in each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify ISOMICRON’s terms and conditions of purchase, including but not limited to the warranty expressed therein.
- Discoloration might be occurred on the package surface after soldering, reflow or long-time use. It neither impacts the performance nor reliability.